Reduction of Input Current Harmonics based on Space Vector Modulation for Three-level Inverter with varied Power Factor

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***Abstract*—This paper presents a novel space vector modulation (SVM) which reduces current harmonics flowing through a DC-link capacitor of a three-level inverter employed for three-phase motor drive systems. In order to reduce the input current harmonics, the space vectors are selected to minimize the difference between the instantaneous value and the average value of the input current by using the magnitude relationships of the output currents. Furthermore, by determining the sector of the proposed SVM from these magnitude relations, the input current harmonics are reduced even when the load power factor changes. The experimental verification clarifies that the proposed SVM reduces the input current harmonics by 24.6% at the power factor of 0.866 and the modulation index of 0.7.**

***Index Terms*—Space vector modulation, Three-level voltage source inverter, Input current harmonics, DC-link capacitor.**

I. Introduction

Recently, three-level voltage source inverters (3LVSIs) are increasingly employed for motor drive systems [1]. 3LVSIs are possible to reduce output voltage harmonics compared to two-level voltage source inverters (2LVSIs) without increasing switching frequency [2]. Consequently, harmonic loss generated in a load motor can be reduced by applying 3LVSIs to motor drive systems as DC-AC converter [3].

Generally, electrolytic capacitors are used as the smoothing capacitor in the DC part of 3LVSI. However, electrolyte easily deteriorates as a result of an exothermic reaction caused by influx of the inverter input current harmonics. Thus, the lifetime of these electrolytic capacitors are critical problem for the lifetime of whole motor drive systems. It is possible to extend the lifetime of these electrolytic capacitors by reducing the inverter input current harmonics.

Heretofore, the modulation method decreases the leakage current of 3LVSIs for PV systems by reducing neutral-point voltage ripple [4]. This modulation method is also possible to reduce the input current harmonics of 3LVSIs only when the load power factor is around unity. Thus, this modulation method cannot be applied to the motor drive systems, the power factor variation of which is considerably wide.

This paper presents a novel space vector modulation (SVM) which reduces the switching-frequency-order harmonics included in the input current of 3LVSI over all range of the load power factor. The proposed SVM reduces the input current harmonics of 3LVSIs by selecting space vectors in order to minimize the difference between the instantaneous value and the average value of the input current of 3LVSI based on the magnitude relationships of the three-phase output currents. The proposed SVM reduces the input current harmonics of 3LVSIs even when the load power factor becomes low by determining the sectors of the proposed SVM from the combination of the three-phase output current's polarities. The reason is that the instantaneous value of the inverter input current depends on the magnitude relationships of the three-phase output currents. Finally, the effectiveness of the proposed SVM is confirmed by simulation and experiment with an induction motor.

II. Space Vector Modulation to Reduce Input Current Harmonics

A. Conventional Three-Level SVM

Fig. 1 shows a T-type 3LVSI. In general, there are two types of 3LVSIs: neutral point clamped (NPC) inverter and T-type inverter. The T-type 3LVSI is considered in this paper because the number of devices in the current path is reduced compared to the NPC inverter, resulting in low conduction losses. It is noted that the modulation methods described below do not depend on the circuit topology of 3LVSI.

Table I shows the relationships between the switching function and the phase voltage of 3LVSI. The switching function of T-type 3LVSI are defined as

$$s_{nj} = \begin{cases} 1, & (\mathrm{S}_{nj} : \mathrm{ON}) \\ 0, & (\mathrm{S}_{nj} : \mathrm{OFF}) \end{cases}, \quad (j = 1,2,3,4) \tag{1}$$

where, n is the output phase and j is the number of switch. Three switching states and three-level phase voltages are available in 3LVSIs.

The output currents of the inverter at steady state are expressed as

$$\begin{cases} i_u = I_m \cos(\theta - \varphi) \\ i_v = I_m \cos\left(\theta - \varphi - \dfrac{2\pi}{3}\right) \\ i_w = I_m \cos\left(\theta - \varphi + \dfrac{2\pi}{3}\right) \end{cases} \tag{2}$$

where, I_m is the maximum value of the output current, θ is the phase angle, and φ is the load power factor angle.

Fig. 2 shows the principle of the conventional three-level SVM. In particular, there are nineteen space vectors ($\mathbf{V_0} \sim \mathbf{V_{18}}$). The $\alpha\beta$ plane where 3LVSI can generate the output voltage is divided into six sectors (sector I ~ VI) in every 60 degrees of the voltage reference vector's phase angle. The voltage reference vector can be expressed with the modulation index (m) and the phase angle as below.

$$\mathbf{V}^* = m\angle\theta \tag{3}$$

Each sector of the conventional three-level SVM can be regarded as the space vector diagram of the two-level SVM. Thus, three-level SVM can be applied in the same way as two-level SVM by defining an inner vector ($\mathbf{V^*_{in}}$) shown as right part in Fig. 2. The inner vector can be obtained by decomposing the voltage reference vector by the equivalent zero vector of two-level SVM in each sector (e.g. $\mathbf{V_7}$ in the sector I) as

$$\mathbf{V}^*_{\mathbf{in}} = V^*_{in}\angle\gamma = \mathbf{V}^* - \mathbf{V}_{\mathbf{6}+i} \tag{4}$$

where, γ is the phase angle of the inner vector and i is the number of sector where the inner vector exists. Each sector of the conventional SVM is also divided into six subsectors (subsector 1 ~ 6) in every 60 degrees of the phase angle of the inner vector. Furthermore, three space vectors surrounding the subsector where the inner vector exists are selected to generate the voltage reference vector. The inner vector sampled in each control period (T_s) is generated by synthesizing these three time-averaged space vectors $\mathbf{V_x}$, $\mathbf{V_y}$, $\mathbf{V_z}$ as

$$\mathbf{V}^*_{\mathbf{in}} = V^*_{in}\angle\gamma = \frac{t_x}{T_s}\mathbf{V}_{\mathrm{x}} + \frac{t_y}{T_s}\mathbf{V}_{\mathrm{y}} + \frac{t_z}{T_s}\mathbf{V}_{\mathrm{z}} \tag{5}$$

$$T_s = t_x + t_y + t_z$$

where, t_x, t_y, t_z are the on duty of each selected space vectors and x, y, z express the number of each selected space vector [5].

B. Evaluation for Input Current Harmonics

Fig. 3 shows the instantaneous waveform of the input current with the conventional SVM. The sampling timing is carried out when the voltage reference vector occurs in sector I and subsector 1 shown as Fig. 2.

Fig. 4 shows the waveforms of the voltage references and the output currents at unity power factor. The instantaneous values of P-side and N-side input current of the T-type 3LVSI are calculated from the switching functions and the output currents as

$$\begin{aligned} i_{DC.in.P} &= \sum_{n=u,v,w}\left(s_{n1}\times i_n\right) \\ i_{DC.in.N} &= \sum_{n=u,v,w}\left(s_{n2}\times i_n\right). \end{aligned} \tag{6}$$

Since the input side of three-phase VSI operates at six-fold fundamental frequency, the rms value of the inverter input current over a sixth of the fundamental period is calculated as

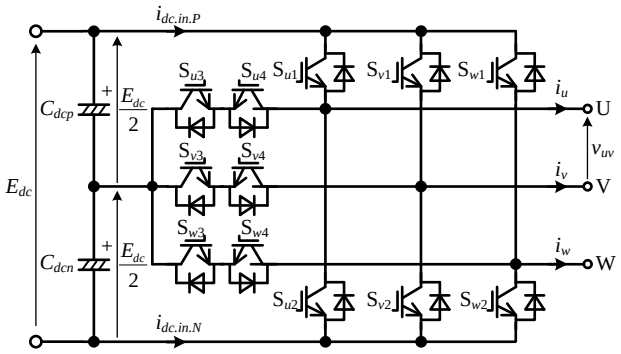


Fig. 1. T-type three-level voltage source inverter.

TABLE I
SWITCHING STATES OF THREE-LEVEL VSI

Switching state	V_{phase} [V]	Switching functions (n = u, v, w)			
		s_{n1}	s_{n2}	s_{n3}	s_{n4}
P (+)	+ E_{dc} /2	1	0	1	0
0	0	0	0	1	1
N (-)	- E_{dc} /2	0	1	0	1

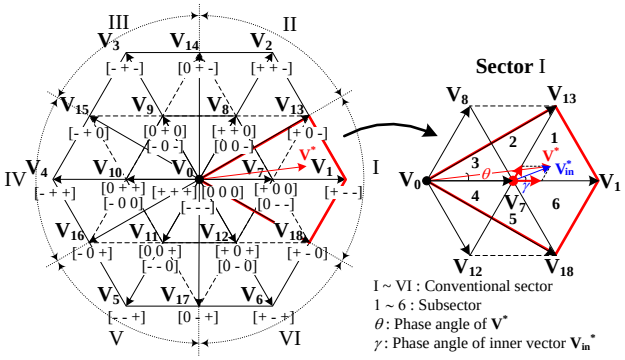


Fig. 2. Conventional three-level SVM.

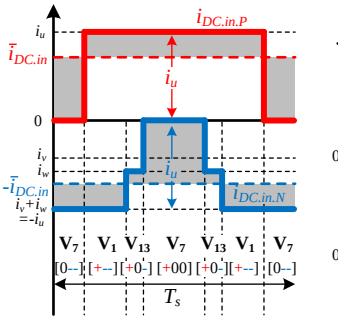


Fig. 3. Instantaneous waveform of input current with conventional SVM.

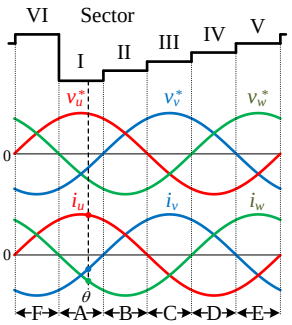


Fig. 4. Waveforms of voltage references and output current at unity power factor.

$$i_{DC.in.RMS} = \sqrt{\frac{3}{\pi}\int_0^{\frac{\pi}{3}}\frac{1}{2}\left(\sum_{k=x,y,z}\frac{t_k}{T_s}\left(i^2_{DC.in.P,k} + i^2_{DC.in.N,k}\right)\right)d\theta} \tag{7}$$

where, t_k is the on duty of the selected space vector and $i_{DC.in.P,k}$, $i_{DC.in.N,k}$ are the instantaneous values of P-side and N-side input current of the T-type 3LVSI when the selected space vector is applied.

Then, the average value of the inverter input current over a sixth of the fundamental period can be calculated as

$$\bar{i}_{DC.in} = \frac{3}{\pi}\int_0^{\frac{\pi}{3}}\left(\sum_{k=x,y,z}\frac{t_k}{T_s}i_{DC.in.P,k}\right)d\theta = \frac{3}{4}m\cdot I_m\cos\varphi\,. \tag{8}$$

The rms value of the current flowing into the smoothing capacitor can be calculated by using (7) and (8) as [6]

$$i_{C.RMS} = \sqrt{i_{DC.in.RMS}^2 - \bar{i}_{DC.in}^2}\,. \tag{9}$$

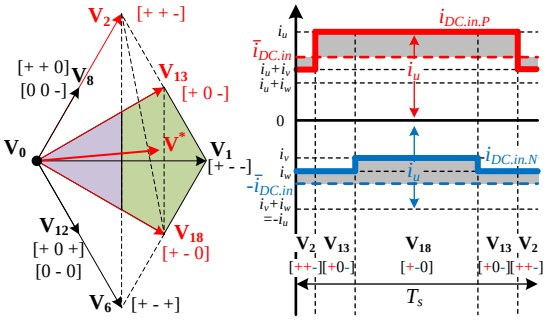
It is understood from (7) that the rms value of the inverter input current changes according to the choice of the space vectors. On the other hand, it is understood from (8) that the average value of the inverter input current does not depend on the choice of the space vectors, but only depends on the modulation index and the load power factor. In other words, the average value of the inverter input current is constant regardless of the choice of the space vectors. Therefore, by selecting the space vectors in order to minimize the rms value of the inverter input current, the rms value of the smoothing capacitor current is also minimized. In order to analyze the optimized vector patterns for the minimum rms value of the inverter input current, the rms value of the inverter input current over a control period named as the instantaneous rms value, derived from (7) as following, is used [7].

$$i_{DC.in.RMS}(T_s) = \sqrt{\frac{1}{2T_s}\int_0^{T_s}\left(i_{DC.in.P}^2 + i_{DC.in.N}^2\right)dt} = \sqrt{\sum_{k=x,y,z}\frac{t_k}{2T_s}\left(i_{DC.in.P,k}^2 + i_{DC.in.N,k}^2\right)} \tag{10}$$

Note that the value of (10) is independent from the switching period because the ratio between the on duty of each space vector and the switching period (t_k/T_s) does not change even when the switching frequency is changed. Therefore, the rms value of the inverter input current is independent from the switching frequency.

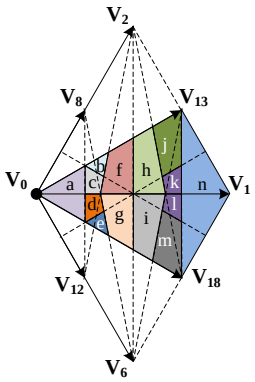
C. Proposed Input Current Harmonics Reduction Method

Fig. 5 shows an example of the instantaneous waveform of the inverter input current with the optimized vector pattern for the minimum instantaneous rms value of the inverter input current when i_u is positive and i_v and i_w are negative. Fig. 5(a) and 5(b) are the examples of the optimized vector pattern for the minimum instantaneous rms value of the inverter input current and the instantaneous waveform of the input current at that moment, respectively. The time integral of the difference between the instantaneous values and the average value of both side input current as shown by the gray areas in Fig. 5(b) with the space vectors **V**$_2$, **V**$_{13}$, **V**$_{18}$ becomes smaller compared to Fig. 3 in which the conventional SVM is applied. The smaller these areas are, the smaller the



(a) One example of optimized vector pattern (**V**$_2$, **V**$_{13}$, **V**$_{18}$). (b) Waveform of input current.

Fig. 5. Instantaneous waveform of input current with the optimized vector pattern for minimum instantaneous rms value of inverter input current when i_u is positive and i_v and i_w are negative.



Area	Vector	Area	Vector
a	**V**$_8$-**V**$_0$-**V**$_{12}$	h	**V**$_2$-**V**$_{13}$-**V**$_6$
b	**V**$_2$-**V**$_8$-**V**$_{12}$	i	**V**$_2$-**V**$_{18}$-**V**$_6$
c	**V**$_8$-**V**$_0$-**V**$_6$	j	**V**$_2$-**V**$_{13}$-**V**$_{18}$
d	**V**$_2$-**V**$_0$-**V**$_{12}$	k	**V**$_{13}$-**V**$_1$-**V**$_6$
e	**V**$_8$-**V**$_{12}$-**V**$_6$	l	**V**$_2$-**V**$_1$-**V**$_{18}$
f	**V**$_2$-**V**$_8$-**V**$_6$	m	**V**$_{13}$-**V**$_{18}$-**V**$_6$
g	**V**$_2$-**V**$_{12}$-**V**$_6$	n	**V**$_{13}$-**V**$_1$-**V**$_{18}$

Fig. 6. Proposed vector patterns to minimize rms value of 3LVSI input current when i_u is positive and i_v and i_w are negative.

instantaneous rms value of inverter input current becomes [8]. As a result, the rms value of the current flowing into the smoothing capacitor can be also reduced by selecting these space vectors. In the high modulation index region shown as the green area in Fig. 5(a), the space vectors which can reduce the instantaneous rms value of the inverter input current are **V**$_2$, **V**$_{13}$, **V**$_1$, **V**$_{18}$ and **V**$_6$. Consequently, the rms value of the inverter input current becomes the minimum by selecting three space vectors from these five space vectors in the high modulation index region. On the other hand, in the low modulation index region shown as the purple area in Fig. 5(a), the rms value becomes the minimum by selecting three space vector from **V**$_2$, **V**$_8$, **V**$_0$, **V**$_{12}$ and **V**$_6$.

Fig. 6 shows the proposed vector patterns to minimize the rms value of the inverter input current when i_u is positive and i_v and i_w are negative. Three space vectors which are the closest to the voltage reference vector are selected for the modulation from these five space vectors which minimize the rms value of the inverter input current.

Moreover, the proposed SVM can control the dc ripple of the neutral-point voltage of 3LVSI. In the proposed vector pattern, at least one output phase is connected to the neutral point of the 3LVSI at any control period. Thus, by applying offset to the voltage references, the difference between the capacitor voltages of the top and bottom smoothing capacitors can still be reduced.

D. Adapting to Variation of Load Power Factor

Table 2 shows the proposed sector definitions to deal with the variation of the load power factor. The sectors of the proposed SVM (A ~ F) are determined by the combination of the polarities of the inverter output currents.

Fig. 7 shows the proposed SVM to minimize the rms value of the 3LVSI input current in low load power factor. The proposed vector patterns shown in Fig. 6 are effective to minimize the rms value of 3LVSI input current only when i_u is positive and i_v and i_w are negative, i.e. the proposed sector A. When the load power factor changes and the magnitude relationships of the output currents changes, it is necessary to deal with that change in order to still be able to minimize the rms value of the 3LVSI input current. In the proposed SVM, by determining the sector from the magnitude relationships of the output currents shown as Table 2, the vector patterns in which the rms value of the 3LVSI input current is minimum at that moment can be applied corresponding to the load power factor change. Note that the detection of the load power factor is unnecessary. In particular, the sectors of the proposed SVM shift corresponding to the load power factor angle (φ) shown as Fig. 7. When the load power factor becomes smaller than 0.5 ($\varphi > 30$ degrees), there are areas which cannot be modulated by the proposed vector pattern to minimize the rms value of the 3LVSI input current and expressed as the shaded areas in Fig. 7. Hence, the conventional SVM is applied in these areas and the proposed vector patterns are applied in other area in the case of the low power factor.

III. Experimental Verifications

The performances of the conventional and proposed SVM are verified in experiment. The switching frequency of the T-type 3LVSI is 10 kHz. In the experiment, a three-phase induction motor (200 V, 1.5 kW, 1500 r/min, MVK8097A, Fuji Electric Co., Ltd.) is used as a test motor. Besides, the load power factor is varied from 0.259 to 0.866, i.e. the case of driving mode, by controlling the torque reference of a load motor.

A. Input Current Harmonic Analysis

In this paper, the input current harmonics of 3LVSI is evaluated as $I_{DC.in(\text{p.u.})}$, which is the rms value of the 3LVSI input current ($I_{DC.in.RMS}$) normalized by the maximum value of the output current (I_m).

$$I_{DC.in(\text{p.u.})} = \frac{I_{DC.in.RMS}}{I_m} = \frac{1}{I_m}\sqrt{\sum_{k=1}^{l}\left(\frac{1}{\sqrt{2}} i_{DC.in,k}\right)^2} \qquad (11)$$

where, k is harmonic order and $i_{DC.in,k}$ is k-order component of the input current harmonics. The fundamental component of the input current harmonics is 50 Hz at rated load. The harmonic components of the input current up to 20th-order of the switching frequency, i.e. up to l-order component of the input current harmonics, are considered in this calculation.

Fig. 8 shows the experimental waveforms of the driving test for the three-phase induction motor at the power factor of 0.866 and the modulation index of 0.7. Fig. 8(a) and 8(b) shows the experimental waveforms with the conventional SVM and proposed SVM, respectively. When the load power factor is high, the applying ratio of the proposed SVM is also high. In particular, the proposed SVM are

TABLE II
SWITHING STATES OF THREE-LEVEL VSI

Sector	Current polarity (P: Positive, N: Negative)		
	i_u	i_v	i_w
A	P	N	N
B	P	P	N
C	N	P	N
D	N	P	P
E	N	N	P
F	P	N	P

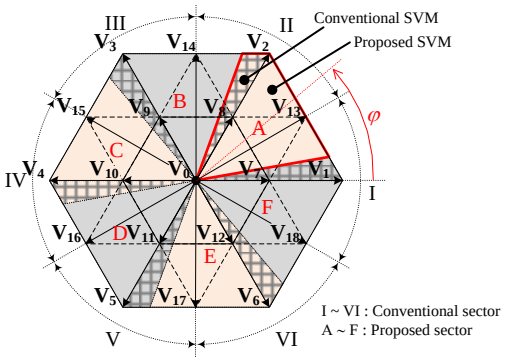
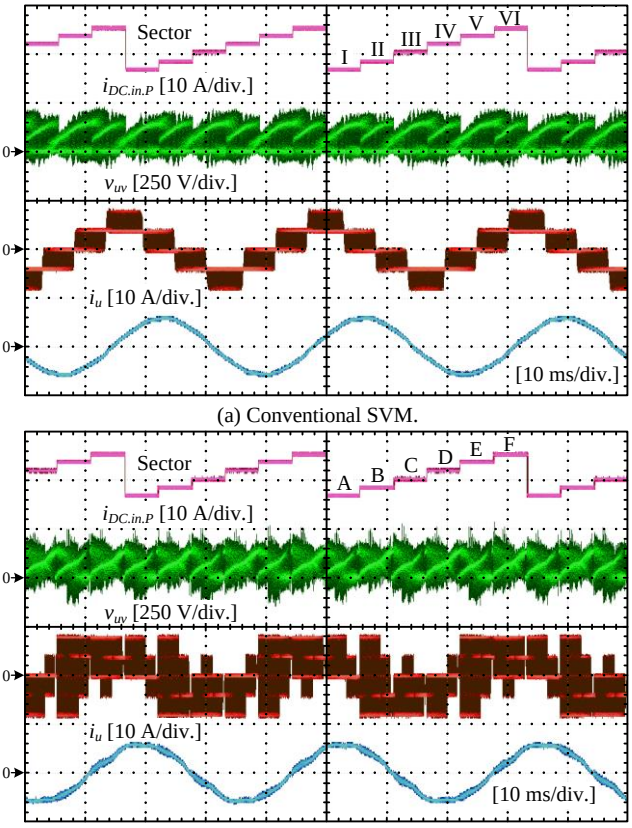


Fig. 7. Proposed three-level SVM when load power factor changes.



(a) Conventional SVM.

(b) Proposed SVM.

Fig. 8. Experimental waveforms at cosφ = 0.866, m = 0.7: Sector, output line voltage, P-side input current, and U-phase output line current.

applied at all time at the load power factor of 0.866. It is confirmed from Fig. 8 that the width of the step change in the input current is reduced by applying the proposed SVM. On the other hand, the distortion of the U-phase output line current with the proposed SVM is slightly higher than the one with the conventional SVM.

Fig. 9 shows the frequency analysis results of the 3LVSI input current at the load power factor of 0.866 and the modulation index of 0.7 (under the same conditions as Fig. 8). Fig. 9(a) and 9(b) are the results with the conventional SVM and proposed SVM, respectively. 100% of the vertical axis implies the maximum value of the output line current, i.e. 6A under this condition. When the conventional SVM is applied, the 3LVSI input current includes large switching frequency-order harmonic component, the value of which is 32.3%. By applying the proposed SVM, the switching frequency-order harmonic component is reduced by 11.7%.

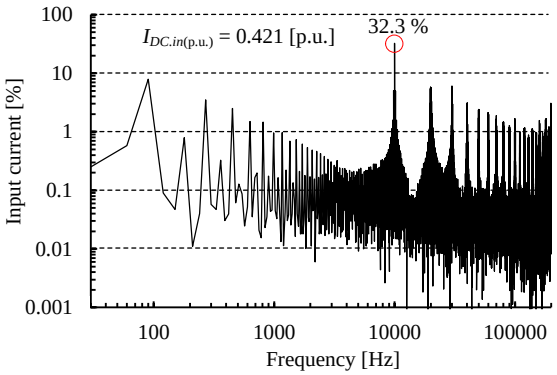
Fig. 10 shows the simulation and experimental results of the analysis of the input current harmonic with the conventional SVM and the proposed SVM. At the power factor of 0.866, i.e. when the load power factor is high, the value of $I_{DC.in(\mathrm{p.u.})}$ is reduced by 24.6% by applying the proposed SVM compared to the case with the conventional SVM. Besides, at the power factor of 0.259, i.e. when the load power factor is low, the value of $I_{DC.in(\mathrm{p.u.})}$ is reduced by 6.55% at most by applying the proposed SVM compared to the case with the conventional SVM. It is also confirmed from this results that as the load power factor becomes smaller, the input current harmonics-reduction effect diminishes because the applying ratio of the proposed SVM is low. Furthermore, the experimental results of $I_{DC.in(\mathrm{p.u.})}$ almost agree with the simulation results. These results confirm that the proposed SVM can reduce the 3LVSI input current harmonics at any load power factor.

B. Output Current Harmonic Analysis

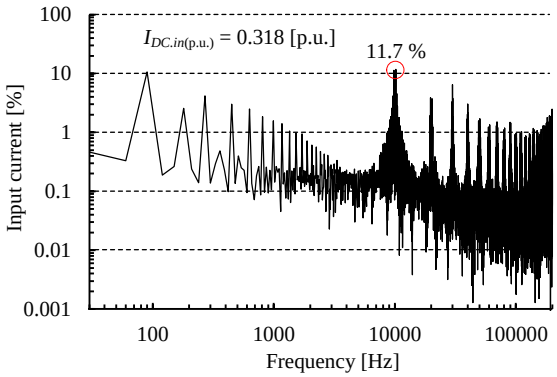
Fig. 11 shows the total harmonic distortion (THD) of the U-phase output line current at the load power factor of 0.866. THD of the output line current is calculated as

$$\mathrm{THD} = \frac{\sqrt{\sum_{k=2}^{40}\left(i_k^2\right)}}{i_1} \qquad (12)$$

where, i_k is k-order component of the output line current harmonics and i_1 is the fundamental component of the output line current harmonics, the rated value of which is 50Hz. THD of the U-phase output line current increases in 2.32 times at most by applying the proposed SVM. In the conventional SVM, three space vectors, the tips of which are the closest to the tip of the voltage reference vector, are selected for modulation. Note that the rms line current ripple can be calculated by using the time integral of the error voltage vector between the applied voltage and reference voltage [9]. Consequently, the conventional SVM is the modulation scheme which achieves low output harmonic. On the other hand, in the proposed SVM, three space vectors, the tips of which are located far

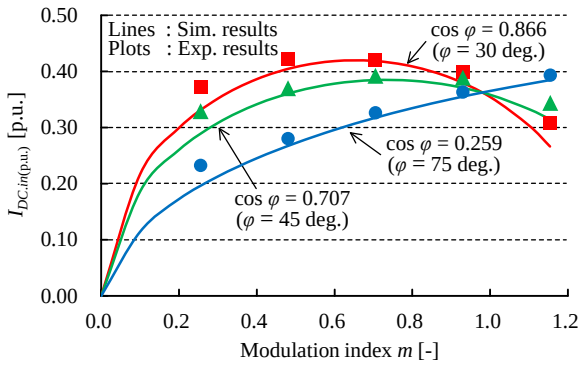


(a) Conventional SVM.

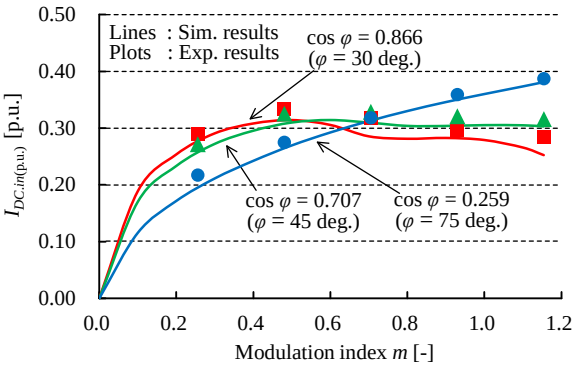


(b) Proposed SVM.

Fig. 9. Frequency analysis results of 3LVSI input current at cos φ = 0.866, m = 0.7 (under the same conditions as Fig. 8). Fundamental frequency is 30 Hz. 100% of vertical axis is the maximum value of output current (6 A).



(a) Conventional SVM.



(b) Proposed SVM.

Fig. 10. Simulation and experimental results of input current harmonics.

from the tip of the voltage reference vector, are selected to minimize the instantaneous rms value of the 3LVSI input current. As a result, THD of the output line current deteriorates when the proposed SVM is applied. However, the increase of the output line current harmonics with the proposed SVM can be simply solved by increasing switching frequency, i.e. shortening the integral time of the error voltage vector between the applied voltage and reference voltage. Meanwhile, the rms value of the 3LVSI input current is independent from the switching period, which implies that the increase in the switching frequency has no influences on the 3LVSI input current harmonics.

IV. Conclusions

In this paper, the novel SVM to reduce the input current harmonics of the 3LVSIs in case that the power factor varies was proposed. This method contributed to the long lifetime of the smoothing capacitor in the motor drive systems. The 3LVSI input current harmonics was reduced by selecting the space vectors to minimize the error between the instantaneous value of the input current and average value by using the magnitude relationships of the output currents. By determining the sector of the proposed SVM from these magnitude relationships, the 3LVSI input current harmonics were reduced even when the load power factor changed.

The effectiveness of the proposed SVM was confirmed by experiments with the induction motor. The experimental results confirmed that the input current harmonics was reduced by 24.6% by applying the proposed SVM. Moreover, it was also confirmed that the input current harmonics was reduced over all range of the power factor. Meanwhile, THD of the output line current deteriorated by applying the proposed SVM because of the selection of the space vectors to reduce the input current harmonics. However, the increase of the output line current harmonics with the proposed SVM can be simply solved by increasing the switching frequency.

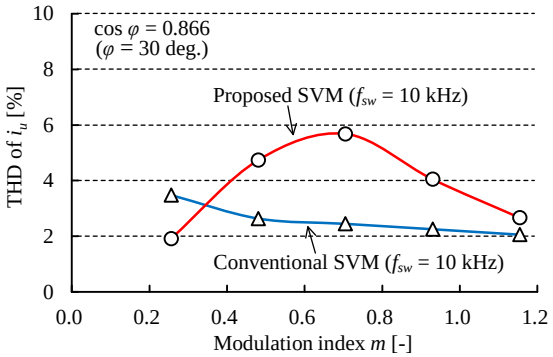


Fig. 11. Total harmonic distortion of output line current with each SVM at power factor of 0.866. f_{sw} is switching frequency.

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